REMARKS

Pending in this Application are Claims 1-24.

Rejections Under 35 U.S.C. 112

Claims 6 and 15

Claims 6 and 15 stand rejected under 35 U.S.C. 112. On page 2 of the Office Action, the Examiner quotes the second paragraph of 35 U.S.C. 112: The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention. In paragraph 2 on page 3 of the Office Action, the Examiner rejected Claims 6 and 15 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as his invention. According to the Examiner, the following statements make the claims indefinite: "the resulting leakage current from said source voltage is approximately 10^{-14} $A/\mu m$". The Examiner states:

The current is defined as amount of charge per cross sectional area (per squared value of length). Citation of current value in amperes per units of length makes the claims indefinite. Accordingly metes and bounds of the claim cannot be determined. The claim has not been treated with regard to prior art.

This rejection has been addressed in amended claims 6 and 15. As noted therein, the leakage current density was cited in terms of Amps/micron *of transistor width*. It is well known in the art of ESD protection that for any device protecting the circuit, the level of protection is proportional to the width of the ESD protection devices. The wider the device, the higher is the level of ESD protection. For example in a typical ESD protection made of one NMOS transistor in a conventional CMOS (no salicide or silicide) operating in snap-back under ESD, the level of protection achieved is of the order of 3KeV/100um of width. For this level of protection, the present invention would have a base leakage of less than 1pA (.01pA/um X 100um). The base leakage is the leakage obtained at point

128 in Figure 2B of the patent application. This leakage is in practice the junction leakage, all sub-threshold transistor leakage having been eliminated by the back-gate bias. A person skilled in the art determines the width of the ESD protecting transistor by knowing which level of protection is required. The leakage achieved in such a case is a function of the selected width at about 0.01pA/um.

On page 8 of the Office Action, Examiner stated that Claims 6 and 15 would be allowable to overcome the cited rejection if they were rewritten to include all of the limitations of the base claim and any intervening claims. Claims 6 and 15 have been amended to overcome the cited rejection as they have been rewritten to include all of the limitations of the base claim and any intervening claims. Thus Claims 6 and 15 should be in a form for allowance.

Rejections Under 35 U.S.C. 102(b)

Claims 1, 5 and 8

Claims 1, 5 and 8 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,903,419 to Smith ("Smith"). On page 3 of the Office Action, Examiner quotes 35 U.S.C. 102(b): A person shall be entitled to a patent unless (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States. In paragraph 3 on page 3 of the Office Action, Examiner states:

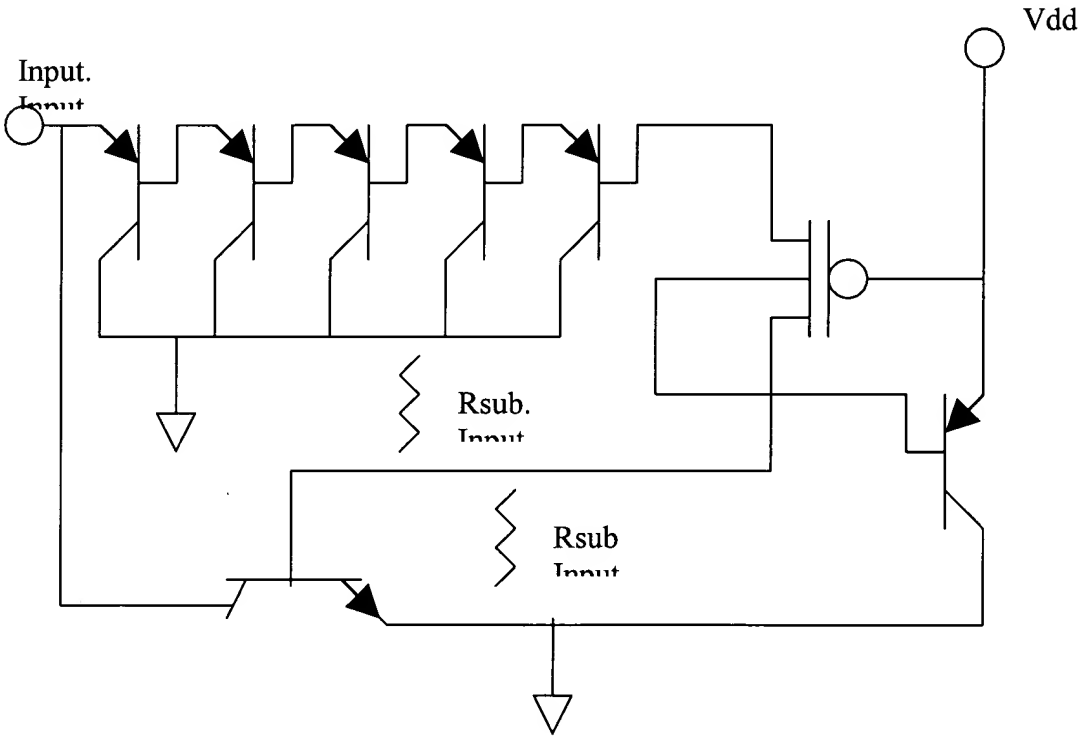
> Smith discloses an ESD protection having a transistor with gate, source, drain and substrate terminals (element 204 in Fig. 2), an input terminal coupled to the source terminal of the transistor (I/0 PAD 14 in Fig. 2), a reference point coupled to the gate and substrate terminals of the transistor (Vdd in Fig. 2), and an output signal terminal coupled to the drain terminal of the transistor (base of transistor 202 is coupled to the drain of transistor 204 in Fig. 2). Due to a diode (element 206 in Fig. 2), a gate to substrate voltage is always positive, which moves the PMOS transistor into sub-threshold regime. Increase of the transistor source voltage reduces the source-to-gate threshold. One of the goals of the invention in the reference is a reduction of a leak current (col. 2, lines 20 - 29, col. 4, lines 1 -5, col. 9, lines 25 -35). Regarding Claim 5, Smith discloses the device having the source voltage of a few hundreds millivolts (a voltage drop across diode 206 in Fig. 2). Regarding Claim 8, discloses a PMOS transistor (element 204 in Fig. 2).

As for Claims 1, 5 and 8, Applicant amends the claims and respectfully traverses the Examiner's rejection and reasoning. Smith discloses an electrostatic discharge (ESD) circuit wherein a discharge path is provided by a parasitic bipolar transistor (202). The parasitic bipolar device is triggered by a combination of a MOSFET (204) and a string of diodes (200). The trigger point of the MOSFET is programmable by varying the number of individual diodes in the string of diodes. A feedback circuit (602) ensures that MOSFET (204) is in a conductive state independent of the voltage state of the voltage supply, VDD, during an ESD event. (see Abstract). As is evident in foregoing description and in the claims of Smith, Smith proposes a concept of ESD protection that does not achieve low current leakage. It is instructive to note that the architecture of Smith is substantially and significantly different than that of the present invention as claimed in Claim 1, 5 and 8.

Smith uses (and relies upon) diodes which it are not possible to have in a regular CMOS process (it is only possible to have a string of parasitic bipolar with common collector) In particular, Smith fails to disclose how to make diodes, or how to select (design) diodes The difficulty with implementing this circuit in a regular CMOS process is that it is not possible to manufacture isolated diodes like those shown above. There are only two ways to obtain diode-like characteristics in a CMOS process, none of which are discussed in Smith.

One way requires special processing to obtain diodes from one of the dielectric-isolated poly-silicon layers. This poly-silicon layer is usually very highly doped to be as conductive as possible. To make a diode out of this layer one needs at least one special mask to prevent the high doping from covering all the poly-silicon. In addition it is not possible to use salicide on the poly unless it too is masked. When used these diodes are very leaky (typically in the nA) and have very high series resistance (Kohms) dues to the poor crystalline structure present in poly-silicon. Smith does not disclose using such diodes nor does he specify anywhere how the diodes are obtained. The second method, presumably the Smith contemplates using on CMOS processes, is to use bipolar transistors. This method only works if the diode is tied to one of the power supply rails otherwise large undesirable collector current will flow to the supply rail (the collector).

In creating a string of diodes like those in Smith and using a regular CMOS process, Smith has created a huge Darlington PNP which base is connected to the PMOS. The base current in this device is the emitter current divided by the current gain to the fifth power, thus with very little current flowing into it. For example with 1 amp of emitter current and a PNP transistor gain of 10 (very low), the base current would be a mere 10uA Making it impossible for this device to trigger the NPN with enough current to shunt the input current. As noted, there is already 1 Amp flowing in the PNP's emitter. (See schematics below):



A bipolar transistor is formed when one attempts to use a N-well and P+ diffusion to create a isolated diode. The reverse bias N-well junction is effectively turning the substrate tie (P-) into a collector. Thus collecting the greatest proportion of the emitter current. Cascading such diode result in a Darlington configuration. Thus, if the 5 diodes of Smith are removed, and the diode connecting the substrate and the gate are tied together, remove the parasitic bipolar and connect the PMOS drain

to Vss, then the invention of Smith is similar to the present invention. However, these changes leave very little of the Smith invention.

Thus, the "stripping" of the Smith patent components as described herein, cannot have been obvious by someone skilled in the art at the time of the present invention as the Smith invention fails to work on CMOS No more than a single MOS transistor properly connected is needed to achieve very low leakage and no degradation of ESD protection for any given technology. Therefore, the added components around a PMOS transistor which does not conduct current under ESD or regular bias would not suggest the present invention.

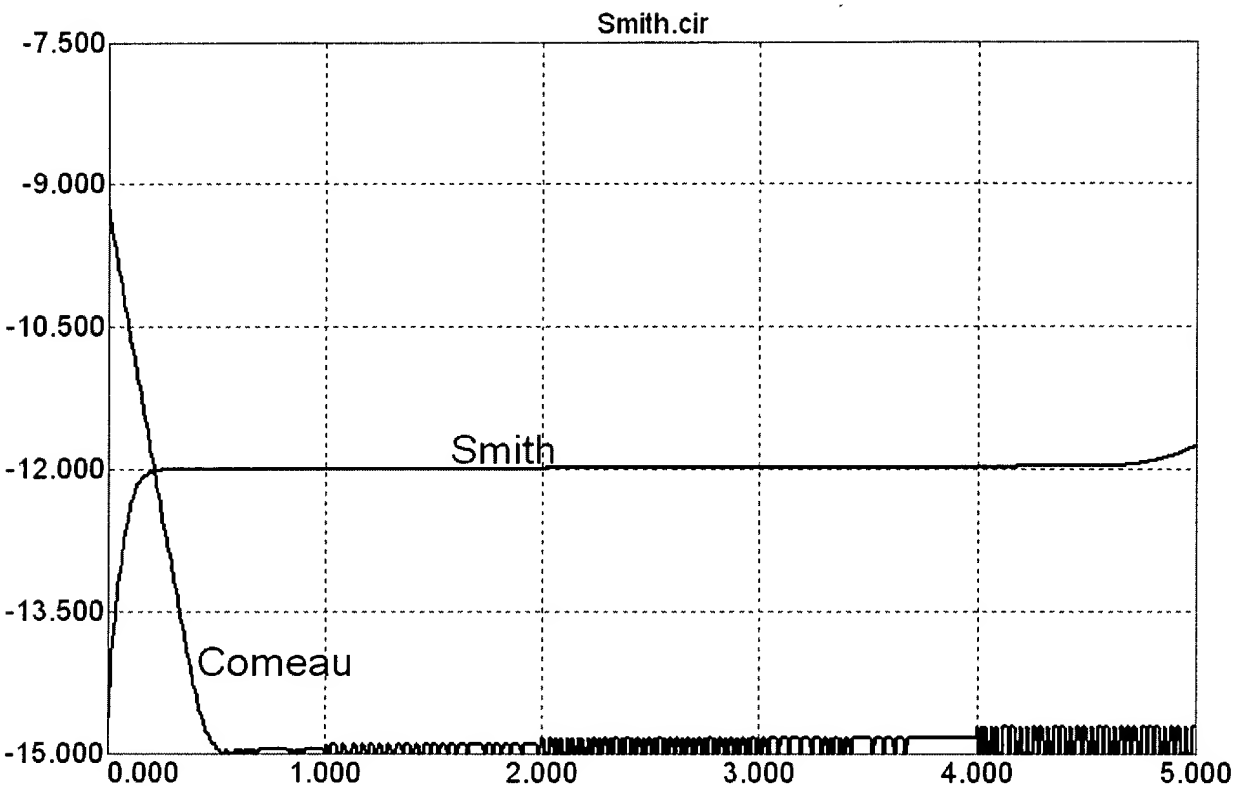
Smith does not propose the concept of using a single MOS transistor, as does the present invention nor does it discuss why the Smith arrangement of transistor and diodes is better than a single transistor from a view point of ESD or from a view point of input leakage. One skilled in the art would be expected to look at the most simple solution first and them improve on it by adding circuitry to address specific problems of the more simple one transistor approach. It is instructive that Smith does not discuss the level of ESD protection achieved. Smith's patent possibly only works on silicon on insulator ("SOI") were it is possible to have all the components required.

The ESD protection circuit of the present invention provides very low leakage and uses only one MOS transistor. Smith's claim to provide low leakage but fails to identify how low is the leakage. Smith's also uses several components (6 diodes, 1 MOS, 1 bipolar in the minimal configuration), the present invention as claimed in the application uses only one transistor, thus requires much less space. The level of ESD protection achieved with the circuit of the present invention is equal to the usual level of protection using the single transistor method described in the prior art for any given CMOS technology. This reduces risk when implementing ESD protection on a new IC where lower input leakage is required. Implementing a totally new approach adds significant risk to such project.

The invention of Smith appears to use isolated diodes 200 (of Smith), however the description in Smith does not disclose how these diodes are constructed. In effect, it is impossible using CMOS technology to create isolated diodes, although they can be fabricated using poly-silicon. Such diodes have high current leakage and very high series resistance, in the KOhm range

typically, which renders them substantially inferior for ESD protection. For example, a 2KeV ESD stress applies a 2.6Amps stress through an input protection device. In order to maintain on-chip voltages below 10-20V, a series resistance of less than 10 Ohms is necessary. The disclosure of Smith does not describe how such low resistance is achieved. As disclosed in the present invention low resistance is obtained because, during the ESD event, the MOS transistor goes into snap-back and possibly secondary snap-back. General ESD protection concepts are not discussed in the present invention as these are well known in the art.

To further illustrate that the invention of Smith is substantially, and significantly different from the present invention, in the Smith invention current must to flow through the PMOS transistor and diodes to provide the reverse bias. Also, the invention of Smith is much more complex inasmuch as the Smith invention requires at least eight (8) components and is sensitive to the manufacturing technology. In contrast, the present invention only requires one (1) components and is not manufacturing technology dependent. In operation, the present invention differs substantially from the present invention. The present invention requires no DC current to bias the I/O protection transistor such that the source junction is reversed biased. As a result, the invention of Smith has leakage much higher than the present invention and thus the Smith invention is not usable in ultra-low-leakage applications. Below is a graph of the simulated I/O protection for the Smith invention and the protection of the present invention. As can be seen, the present invention as claimed in Claims 1, 5 and 8 perform much better from a leakage view point.



For a prior-art reference to anticipate under 35 U.S.C. Section 102, every element of the claimed invention must be identically shown in a single reference. These elements must be arranged as in the claimed under review. *In re Bond*, 15 U.S.P.Q.2d 1566, 1567-68 (Fed. Cir. 1990). As such, Smith cannot anticipate Claim 1 or any of its respective dependent claims, including Claims 5 and 8.

Rejections Under 35 U.S.C. 103(a)

Claims 7, 2, 3 and 4

Claims 7, 2, 3, and 4 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Smith in view of the A. Sedra and K. Smith textbook "Microelectronic Circuits" ("Sedra Textbook"). Examiner quotes 35 U.S.C. 103(a):

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

In paragraph 4 on page 4 of the Office Action, Examiner states:

> Smith discloses all the elements of Claim 1. However, regarding Claim 7, it does not disclose the NMOS transistor. According to the Microelectronic Circuits textbook (pages 3442 -343), the NMOS and PMOS transistors are equivalents and are interchangeable. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used NMOS transistor as equivalent replacement for PMOS transistor, because as the textbook states (pages 243 -343), they are equivalents and interchangeable. Selection of particular type of transistor is a designer decision, which is far from being an inventive step.

As for Claims 7, Applicant respectfully traverses the Examiner's rejection and reasoning. As noted above, Smith does not disclose all the elements of Claim 1. Smith discloses an electrostatic discharge (ESD) circuit wherein a discharge path is provided by a parasitic bipolar transistor (202). The parasitic bipolar device is triggered by a combination of a MOSFET (204) and a string of diodes (200). The trigger point of the MOSFET is programmable by varying the number of individual diodes in the string of diodes. A feedback circuit (602) ensures that MOSFET (204) is in a conductive state independent of the voltage state of the voltage supply, VDD, during an ESD event. (see Abstract). As is evident in foregoing description and in the claims of Smith, Smith proposes a concept of ESD protection that does not achieve low current leakage. It is instructive to note that the architecture of Smith is substantially and significantly different than that of the present invention as claimed in Claim 1, from which Claim 7 depends.

Further, regarding Claims 2, 3 and 4, the Examiner states:

> Smith discloses the reference point (element Vdd in Fig. 2), which for PMOS transistor plays the same role as the ground, or Vss (the lowest potential) voltage for NMOS transistor. Therefore, for the equivalent PMOS transistor the reference potential is equal Vdd volts, rather than 0 volts.

As for Claims 2, 3 and 4, Applicant respectfully traverses the Examiner's rejection and reasoning. As noted above, Smith does not disclose all the elements of Claim 1. The architecture of Smith is substantially and significantly different than that of the present invention as claimed in Claim 1, from which Claims 2, 3 and 4 depend.

Combination of References

The **combination** of Smith and the Sedra Textbook fails to render the claimed invention in Claims 7, 2, 3 and 4 obvious. The architecture and objectives of the Smith invention are significantly and substantially different from that claimed in Claims 7, 2, 3 and 4. Furthermore, neither invention of Smith, nor the general interchangeability of PMOS transistors and NMOS transistors as described in the Sedra Textbook gives rise to any suggestion or incentive in either reference to combine the references so as to arrange the elements in the manner described in Claim 1, from which claims 7, 2, 3 and 4 depend. Thus, without using hindsight of selective picking and choosing, Applicant respectfully submits that the combination of the references falls short of rendering obvious the claimed invention.

In discussing a rejection under 35 U.S.C. 103, the Court, in *In re Wesslau*, 147 U.S.P.Q. 391, 393 (C.C.P.A. 1965) held that:

It is impermissible within the framework of Section 103 to pick and choose from any one reference only so much of its as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art.

The Examiner may not use Applicant's claims as a blueprint to pick and choose from one of the references only so much of it as will support the Examiner's position and to exclude other parts necessary to the full appreciation of what that reference fairly suggests to one of ordinary skill in the art. This type of piecemeal reconstruction of the references in light of Applicant's disclosure is not a permissible basis for holding the invention obvious. *In re Kamm and Young*, 172 U.S.P.Q. 298, 301-302 (C.C.PA. 1972).

The Federal Circuit has repeatedly held that hindsight must be avoided in combining reference structures. *Panduit Corp. v. Dennison Manufacturing Co.*, 227 U.S.P.Q. 337, 343 (Fed. Cir. 1985); *In re Find*, 5 U.S.P.Q.2d 1596, 1599-1560 (Fed. Cir. 1988). Thus, it is error to reconstruct a patentee's claimed invention from the prior art by using the patentee's claims as a blueprint. Prior art references must be read as a whole and consideration must be given where the references diverge and teach away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 220 U.S.PQ. 303, 311-13 (Fed. Cir. 1983). A claim cannot properly be used as a blueprint for abstracting individual teachings from references. *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 227 U.S.P.Q. 657, 667 (Fed. Cir. 1985).

Claims 9, 14, 17, 18, 20 and 22-24

Claims 9, 14, 17, 18 and 22-24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Watt et al. (U.S. Pat.No. 5,751,507) ("Watt") in view of Smith. Regarding Claims 9 and 18, Examiner states:

> ...Watt et al. discloses an ESD protection solution for a plurality of low operating voltage devices having a plurality of input terminals (input pads 1, 2, ... N in Fig. 2). Each input has its own ESD protection (elements D1 and D3 in Fig. 2).
>
> However, he does not disclose a low leakage current solution for ESD protection devices. Smith discloses an ESD protection having a transistor with gate, source, drain and substrate terminals (element 204 in Fig. 2), an input terminal coupled to the source terminal of the transistor (I/0 PAD 14 in Fig. 2), a reference point coupled to the gate and substrate terminals of the transistor (Vdd in Fig. 2), and an output signal terminal coupled to the drain terminal of the transistor (base of transistor 202 is coupled to the drain of transistor 204 in Fig. 2). Due to a diode (element 206 in Fig. 2), a gate to substrate voltage is always positive, which moves the PMOS transistor into subthreshold regime. Increase of the transistor source voltage reduces the source-to-gate threshold. One of the goals of the invention in the reference is a reduction of a leak current (col. 2, lines 20 - 29, col. 4, lines 1 -5, col. 9, lines 25 -35). Both patents have the same problem solving area, namely providing an efficient ESD protection for integrated circuits. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the plurality of transistors according to Smith protecting each of the inputs of the Watt et al. circuit, because as well known in the art and stressed by Smith (col. 2, lines 20 - 29), the leakage current presents a problem in many electronic circuits, especially in a view that they increase with a temperature.

As for Claims 9 and 18, Applicant respectfully traverses the Examiner's rejection and reasoning. Claim 18 of the present invention provides:

> 18. (currently amended) A low voltage CMOS Integrated Circuit (IC) with on-board ESD input protection comprising:
>
> a plurality of low operating voltage devices,
>
> at least one reference point, one supply voltage point and a plurality of input terminals coupled to said devices;
>
> a plurality of input paths for coupling input signals to said devices via said input terminals; and
>
> a plurality of input protection transistors with gate, substrate, source, and drain terminals arranged between said input paths and said devices, each source terminal coupled to a corresponding input path, each gate and substrate terminal coupled to a reference point;
>
> wherein a leakage current of said input protection transistors is controlled to a sub-threshold level over a range of voltages applied to each source terminal of said input protection transistors.

The description and operation of the Smith invention is described above. The analysis and differentiation of the Smith invention under the discussion of Claims 1, 5, and 8 of the present invention are incorporated herein by reference. Watt discloses an apparatus for protecting an integrated circuit against damage from electrostatic discharges (ESD), which includes a single ESD bus that is connected to multiple input pads through a respective diode. The ESD bus is isolated from the positive power supply bus V_{DD}. The ESD bus is coupled to the negative power supply bus Vss by a FET-triggered SCR circuit. ESD charge on an input pad forward biases the respective diode and charges the ESD bus. When the voltage of the ESD bus reaches a predetermined threshold voltage, the FET breaks down, and triggers the SCR circuit to shunt the charge on the ESD bus to V_{SS}. The

threshold voltage is selected such that, in normal operation, voltages higher than V_{DD} may be applied to the input pad without input leakage current.

The **combination** of Smith and Watt fails to render the claimed invention in Claims 9 and 18 obvious. Smith does not disclose all the elements of Claim 9 or Claim 18. The architecture and objectives of Smith are substantially and significantly different than that of the present invention as claimed in Claims 9 and 18. Furthermore, neither invention of Smith, nor the invention of Watt give rise to any suggestion or incentive in either reference to combine the references so as to arrange the elements in the manner described in Claims 9 or 18. The case law interpreting the proper use of references for 35 U.S.C. 103(a) purposes as set forth under the discussion of Claims 7, 2, 3 and 4 of the present invention is incorporated herein by reference. Thus, without using hindsight of selective picking and choosing, Applicant respectfully submits that the combination of the references falls short of rendering obvious the claimed invention.

Regarding Claim 14, Examiner states:

Smith discloses the device having the source voltage of a few hundreds millivolts (a voltage drop across diode 206 in Fig. 2).

Claim 14 of the present invention provides:

> 14. (original) The protection scheme of claim 9 wherein said source voltage is limited to a few 100mV.

As for Claim 14, Applicant respectfully traverses the Examiner's rejection and reasoning. Applicant respectfully suggest here that it has demonstrated that Smith does not work for CMOS and that it would not have been obvious for one skilled in the art at the time of Smith's invention that his invention did not work for CMOS,. As such, the **combination** of Smith and Watt fails to render the claimed invention in Claim 14 obvious. The architecture and objectives of the Smith invention are significantly and substantially different from that claimed in Claim 14. The analysis and differentiation of the Smith invention under the discussion of Claims 1, 5, and 8 of the present invention are incorporated herein by reference. Furthermore, neither invention of Smith, nor the

invention of Watt gives rise to any suggestion or incentive in either reference to combine the references so as to arrange the elements in the manner described in Claim 14. The case law interpreting the proper use of references for 35 U.S.C. 103(a) purposes as set forth under the discussion of Claims 7, 2, 3 and 4 of the present invention is incorporated herein by reference. Thus, without using hindsight of selective picking and choosing, Applicant respectfully submits that the combination of the references falls short of rendering obvious the claimed invention.

Claim 10

Claim 10 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Watt et al. in view of Smith and further in a view of Ker et al. article "Capacitor-Coupled ESD Protection Circuit for Deep-Submicron Low-Voltage CMOS ASIC" (the "Ker Article"). In paragraph 6 on page 6 of the Office Action, the Examiner states:

> As was stated above, Watt et al. and Smith disclose all the elements of Claim 9. However, regarding Claim 10, they do not disclose the solution according to teachings of Watt et al. and Smith being used for protection of the low voltage CMOS circuit. Ker et al. discloses an ESD protection for the low voltage CMOS circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the solution according to teachings of Watt et al. and Smith for protection of the low voltage CMOS circuit, because as Ker et al. state (see Operating Principles pages 310- 311), the submicron low voltage CMOS circuits more than other circuits need the ESD protection.

As for Claim 10, Applicant respectfully traverses the Examiner's rejection and reasoning. As noted above, Watt and Smith fail to disclose all the elements of Claim 9, from which Claim 10 depends. The analysis and differentiation of the Smith invention under the discussion of Claims 1, 5, and 8 of the present invention are incorporated herein by reference. Further, the Ker Article proposes a capacitor-coupled technique used to lower snapback-trigger voltage and ensure uniform ESD current distribution in deep-submicron CMOS on-chip ESD protection circuit. The coupling capacitor is realized by a poly layer under the wire-bonding metal pad without increasing extra layout area to the pad. A timing-original design model has been derived to calculate the capacitor-couple efficiency of the Ker proposed ESD protection circuit. According to Ker, using this

capacitor-coupled ESD protection circuit, the thinner gate oxide of CMOS devices in deep-submicron low-voltage CMOS ASIC can be effectively protected. None of the invention of Smith, Watt or the Ker Article gives rise to any suggestion or incentive in any of such reference to combine the references so as to arrange the elements in the manner described in Claims 9 or 10. The case law interpreting the proper use of references for 35 U.S.C. 103(a) purposes as set forth under the discussion of Claims 7, 2, 3 and 4 of the present invention is incorporated herein by reference. Thus, without using hindsight of selective picking and choosing, Applicant respectfully submits that the combination of the references falls short of rendering obvious the claimed invention.

Claims 11-13, 16, 19, 17, 20 and 22-24

Claims 11-13, 16, 19, 17, 20 and 22-24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Watt in a view of Smith and further in view of the Sedra Textbook. In paragraph 7 on page 7 of the Office Action, the Examiner states:

> As was stated above, Watt et al. and Smith disclose all the elements of Claim 9. However, regarding Claims 16 and 19, they do not disclose the NMOS transistor. According to the Microelectronic Circuits textbook (pages 3442 -343), the NMOS and PMOS transistors are equivalents and are interchangeable. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used NMOS transistor as equivalent replacement for PMOS transistor, because as the textbook states (pages 243 -343), they are equivalents and interchangeable. Selection of particular type of transistor is a designer decision, which is far from being an inventive step.

As for Claims 11-13, 16, 19 and 22-24, Applicant respectfully traverses the Examiner's rejection and reasoning. Watt and Smith fail to disclose all the elements of Claim 9, from which Claims 16, and 11-13 depends. The analysis and differentiation of the Smith invention under the discussion of Claims 1, 5, and 8 of the present invention are incorporated herein by reference. Further, as noted above, the inventions of Smith and Watt are significantly and substantially different from the present invention, both in their architectures and in operation Therefore, the further element regarding the interchangeability of NMOS and PMOS, coupled to the foregoing references does not support a given position, to the exclusion of other parts necessary to the full

appreciation of what such reference fairly suggests to one of ordinary skill in the art. The case law interpreting the proper use of references for 35 U.S.C. 103(a) purposes as set forth under the discussion of Claims 7, 2, 3 and 4 of the present invention is incorporated herein by reference. Without using hindsight of selective picking and choosing, Applicant respectfully submits that the combination of the references falls short of rendering obvious the claimed invention.

Regarding Claims 17 and 20, Examiner states: [Smith] "discloses a PMOS transistor (element 204 in Fig. 2)."

Claims 17 and 20

As for Claims 17 and 20, Applicant respectfully traverses the Examiner's rejection and reasoning.

Claim 17 provides:

17. (currently amended) The protection scheme of claim 15 wherein said plurality of transistors are PMOS type.

Claim 20 provides:

20. (original) The IC of claim 18 wherein said plurality of input protection transistors are PMOS type.

The **combination** of Smith and Watt fails to render the claimed invention in Claims 17 (which depends on Claim 9) or 20 (which depends on Claim 18) obvious. The architecture and objectives of the Smith invention are significantly and substantially different from that claimed in Claims 17 and 20. The analysis and differentiation of the Smith invention under the discussion of Claims 1, 5, and 8 of the present invention are incorporated herein by reference. Furthermore, neither invention of Smith, nor the invention of Watt gives rise to any suggestion or incentive in either reference to combine the references so as to arrange the elements in the manner described in Claims 17 or 20. The case law interpreting the proper use of references for 35 U.S.C. 103(a) purposes as set forth under the discussion of Claims 7, 2, 3 and 4 of the present invention is incorporated herein by reference. Thus, without using hindsight of selective picking and choosing, Applicant respectfully submits that the combination of the references falls short of rendering obvious the claimed invention.

Claims 11-13 and 22-24

Claims 11-13 and 22-24 further stand rejected under 35 U.S.C. 103(a) as being unpatentable over Watt in a view of Smith and further in view of the Sedra Textbook. In paragraph 7 on page 8 of the Office Action, the Examiner further states:

> Regarding Claims 11-13 and 22-24, Smith discloses the reference point (element Vdd in Fig. 2), which for PMOS transistor plays the same role as the ground, or Vss voltage for NMOS transistor. Therefore the reference potential is equal Vdd volts, rather than 0 volts.

As for Claims 11-13 and 22-24, Applicant respectfully traverses the Examiner's rejection and reasoning. The analysis and differentiation of the Smith invention under the discussion of Claims 1, 5, and 8 of the present invention are incorporated herein by reference. Watt and Smith fail to disclose all the elements of Claim 9, from which Claims 11-13 depend, and Claim 18 from which Claims 11-13 depend. Further, as noted above, the inventions of Smith and Watt are significantly and substantially different from the present invention, both in their architectures and in operation Therefore, the fact that Smith discloses that the reference potential is equal to Vdd volts, rather than 0 volts, coupled to the foregoing references does not support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art. The case law interpreting the proper use of references for 35 U.S.C. 103(a) purposes as set forth under the discussion of Claims 7, 2, 3 and 4 of the present invention is incorporated herein by reference. Without using hindsight of selective picking and choosing, Applicant respectfully submits that the combination of the references falls short of rendering obvious the claimed invention.

Conclusion

Applicant respectfully submits that Claims 1-24, now pending, are in condition for allowance. A Notice of Allowance is therefore requested.

If the Examiner has any other matters which pertain to this Application, the Examiner is encouraged to contact the undersigned to resolve these matters by Examiner's Amendment where

possible.

Favorable consideration of the pending claims is respectfully requested.

Respectfully Submitted,

Michael G. Cameron
Reg. No. 50, 298

Date: 11-20-03

Jackson Walker L.L.P.
2435 North Central Expressway, Suite 600
Richardson, TX 75080
Tel: (972) 744-2934
Fax: (972) 744-2909